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EXAMINER	
RILEY, MARCUS T	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,886	TAYLOR ET AL.	
	Examiner	Art Unit	
	MARCUS T. RILEY	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/15/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to applicant's remarks received on May 1, 2008. **Claims 1-7** remain pending.

Response to Arguments

2. Applicant's arguments with respect to amended **claims 1-3 & 5,** and newly added **claim 7** filed on May 1, 2008 have been fully considered but they are not persuasive.

A: Applicant's Remarks

Rejections Under 35 U.S.C. § 103

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curry et al. (US 6,112,275) in combination with Smith et al. (US 6,762,733). The applicants respectfully traverse the rejection for at least the following reasons.

Claim 1 has been amended and is now is directed towards a programmable interface that includes, among other features:

a microcontroller configured to bidirectionally communicate with the register file and the run control register;

a Code Store SRAM configured to bidirectionally communicate with the microcontroller;

... the run control register are configured to bidirectionally communicate with a system processor.

Thus, the claim recites a run control register to bidirectionally communicate with a microcontroller and a system processor. For example, the applicants' Fig. 1 illustrates a run control register 16 communicating with main system CPU 30 and microcontroller 12. Such a configuration has certain advantages, some of which are disclosed in the applicants' specification, e.g., paragraph 14, lines 4-5; and paragraph 02, lines 7-8.

The Examiner appears to allege that Curry discloses microcontrollers 2414 and 2404 in Fig. 24 and the Master microprocessor of Fig. 37A, where the Master microprocessor of Fig. 37A bidirectionally communicates with a 1-3 wire convertor, which includes a ROM and control 2108 (Curry, col. 64, lines 53-58). The Examiner appears to equate the Master microprocessor and the ROM and control 2108 (included in the 1-3 wire convertor) with the recited microcontroller and the Code Store SRAM, respectively.

The Examiner acknowledges that Curry does not disclose a run control register; and also does not disclose the run control register configured to bidirectionally communicate with a system processor, but alleges that Smith does disclose these elements. Specifically, the Examiner appears to equate Smith's registers 160, 162, and 164 (coupled to the NVRAM controller 170 or EEPROM controller 172, Fig. 7) to the recited run control register. It is unclear to the applicants where Smith discloses that the registers 160, 162, and 164 correspond to a run control register that communicates with a system processor. A person of ordinary skill in the art would appreciate the difference between a memory controller (e.g., Smith's NVRAM controller 170 or EEPROM controller 172) and the recited system processor. Although Smith's registers 160, 162, and 164 communicate with a memory controller (NVRAM controller 170 or EEPROM

controller 172), Smith does not disclose registers 160, 162, and 164 bidirectionally communicating with a system processor, as required by claim 1.

Additionally, the Examiner alleges that it would be obvious to combine Smith's teaching (registers 160, 162, and 164 communicating with the memory controller) with Curry's system (Master microprocessor of Fig. 37A) to achieve the claimed invention, the motivation for combining being permitting hotel quests to actively participate in video .game play or to use other data processing communication service. The applicants fail to understand how such motivation may be used to combine Smith's teaching with that of Curry to arrive at the specific claimed features. Permitting hotel guests to actively participate in video game play or to use other data processing/communication service does not specifically require configuring Smith's registers 160, 162, and 164 (the alleged run control register) to communicate with Curry's Master microprocessor of Fig. 37A (the alleged microcontroller). It is not simply a matter of the presence of all the claimed elements in the art, but rather an explanation of how one of ordinary skill in the art would be motivated to make the specific combination of reference elements to achieve the claimed configuration. It appears that the Examiner's attempt to combine the elements of the references amounts to improper hindsight reconstruction using applicants' disclosure as a roadmap to arrive at the claimed features. And hence, neither Curry nor Smith, either alone or in combination, disclose or even suggest a run control register that bidirectionally communicates with a microcontroller and a system processor.

Further, claim 1 has been amended to clarify that the system processor is ... configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code. As previously discussed, neither Smith nor Curry,

either alone or in combination, disclose or even suggest a run control register coupled to a system processor and a microcontroller. For at least the same reason, neither of the two cited references, alone or in combination, discloses or suggests that the system processor signals the microcontroller via the run control register to begin execution of one or more instructions, as recited in claim 1.

Moreover, claim 1 recites

a Code Store SRAM configured to bidirectionally communicate with the microcontroller;

executable code, loaded onto the Code Store SRAM;

... the system processor is configured to load the executable code onto the Code Store SRAM ...

As previously discussed, the Examiner appears to equate Curry's Master microprocessor and ROM and control 2108 (included in the 1-3 wire convertor) of Fig. 37A with the recited microcontroller and the Code Store SRAM., respectively. Additionally, the Examiner cites the following to allege that Curry discloses the recited loading of the executable code in the SRAM:

"Counter 2810 can be read over the 1-wire bus by a host in a manner similar to reading the RAM of module 2100: the host resets module 2800 (counter 2810 does not reset except by a command in the command register), and then loads the Read Counter command into the command register and then reads the contents of counter 2810." (Col. 57, lines 26-32).

It appears that the Examiner is now equating Curry's loading of the read counter command in the command reqister to the recited executable code, loaded onto the Code Store SRAM. That is, now the Examiner is equating curry's command register with the recited Code Store SRAM. On the other hand, the Examiner had earlier equated Curry's ROM and control

2108 with the recited Code Store SRAM. Put differently, the Examiner equates two different components (ROM and control 2108, and command register) of Curry with the recited Code Store SRAM while discussing two different features of the Code Store SRAM. And hence, the Examiner has failed to identify a Code Store SRAM in Curry that communicates with the microcontroller and is loaded with executable code.

For at least these reasons, the applicants respectfully submit that neither Curry nor Smith, alone or in combination, discloses or even suggests claim 1, and accordingly, claim 1 is in condition for allowance, along with associated dependent claims 2-6.

New Claim

New claim 7 has been added, which is directed towards a programmable interface that includes, among other features, a system processor that is configured to bidirectionally communicate with the register file. Note that claim 1, from which new claim 7 depends, recites a microcontroller configured to bidirectionally communicate with the register file... Thus, claim 7 recites a register file that bidirectionally communicates with a system processor and a microcontroller.

While rejecting claim 1, the Examiner alleges that Curry's protocol registers 920 of Figs. 9A and 9B disclose the recited register file. Curry's protocol registers 920, however, do not communicate with a system processor (the protocol registers 920 do not even communicate with a microcontroller). Further, in the office action, the Examiner has identified several other registers (e.g., command register of module 2400 communicating with the microcontroller 2404

of Fig. 24). Curry, however, does not disclose a register file that bidirectionally communicates with a system processor and a microcontroller.

A: Examiner's Response

Rejections Under 35 U.S.C. § 103

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curry et al. (US 6,112,275) in combination with Smith et al. (US 6,762,733). The examiner respectfully maintains the rejection for at least the following reasons.

Claim 1 has been amended to include wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.

Smith '733 discloses wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code (*"The bits stored in the respective registers are input to a pseudo RAM (PSRAM) controller 166 which, in turn, selects in accordance with the state of the output from registers 158-164, the pseudo RAM 174 address mapping mode. The address mapping functions implemented by the PSRAM controller 166 permits diverse games using different address mapping modes to be executed using the same memory board hardware."* column 13, lines 3-11).

Smith '733 does disclose a run control register; and also does not disclose the run control register configured to bidirectionally communicate with a system processor.

Smith '733 discloses a run control register (*"The registers 160, 162 and 164 are also coupled to a non-volatile RAM controller 170 which generates a chip select signal for non-volatile RAM 178. Non-volatile RAM 178 is addressed from the SNES address bus and receives write control signal and read control via chip enable as shown in FIG. 7. The contents of boot /run register 164 as well as SNES reset and ROM select signals are coupled to EPROM controller 172 which generates a chip select signal at the appropriate time to read the EPROM 180."* column 13, lines 32-40); wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor (*"As shown in FIG. 6 various power lines and bidirectional control lines are also coupled to the memory board..."* column 11, lines 54-56). (*"The registers 160, 162 and 164 are also coupled to a non-volatile RAM controller 170 which generates a chip select signal for non-volatile RAM 178. Non-volatile RAM 178 is addressed from the SNES address bus and receives write control signal and read control via chip enable as shown in FIG. 7. The contents of boot /run register 164 as well as SNES reset and ROM select signals are coupled to EPROM controller 172 which generates a chip select signal at the appropriate time to read the EPROM 180. The EPROM controller 172 receives an address from the Super NES address bus. The EPROM may be written in response to an SNES write control signal. Each of the pseudo-static RAM 174, SRAM 176, non-volatile RAM 178 and boot ROM 180 is coupled to the SNES address and data buses."* column 13, lines 32-45).

To permit one to *"...use other data processing/communication services"* is sufficient motivation to combine the reference to achieve the claimed configuration.

Thus, Examiner respectfully submit that Curry and Smith, alone or in combination, teaches, disclose or suggests claim 1. Accordingly, claim 1 is in not condition for allowance, along with associated dependent claims 2-7.

New claim 7 has been added, which is directed towards a programmable interface that a system processor that is configured to bidirectionally communicate with the register file.

Regarding claim 7; Smith '733 discloses a device wherein the system processor is configured to bidirectionally communicate with the register file (*"The computer and memory board are also interconnected via an 8 bit address bus PA0-PA7 which permits addressing of registers (described below) that are located in a particular CPU address space."* column 12, lines 26-29). See also (*"Commands from the host computer 7 are coupled to the memory board microcontroller and the SNES (which in turn respond to the host computer 7), via this bidirectional link."* column 12, lines 43-46).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 1-3 & 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Curry et al. (US 6,112,275 hereinafter, Curry '275) in combination with Smith et al. (US 6,762,733 B2 hereinafter, Smith '733).

Regarding claim 1; Curry '275 discloses a programmable interface comprising (*"The presently preferred embodiment also uses an electrical interface to the tokens, which permits interfacing to tokens with a wide variety of computers, including a tremendous variety of personal or other computers, as long as the computer includes an interface to RS232 (or some comparable standard). The token has a one-wire-bus interface, implemented in a battery-backed open-collector architecture, which provides a read/write interface. The communication protocol expected by the token has been specified so that the token never sources current to the data line, but only sinks current. The communication protocol also includes time-domain relations which are referenced to a very crude time base in the token, and the system must preserve timing relations which will be satisfied by tokens in which the time base takes on any of the wide range of foreseeable speeds. To interface to this protocol, the programmable capabilities of the standard UART chip in the computer's RS232 interface are exploited to provide adaptation to the time base requirements of the module."* column 10, lines 3-22): a register file having a plurality of registers, each register having a type (*"FIGS. 9A and 9B are two parts of a single Figure which shows the control logic used, in the presently preferred embodiment, in the integrated circuit of FIG. 6. After the protocol register 920 has been loaded, counter chain 910 counts successive clock pulses. (Every falling edge on the data line will lead to a clock pulse within the module, and these pulses are counted by counter 920.) The counter 910 is also connected to logic which will intercept the clock signal (to freeze the count), and activate signal 210, as soon as 256 bits of data have been read or written. (Note that the counter chain shown actually includes two more stages than are needed. This permits ready modification for 1024-bit embodiments.) Register 920 receives the protocol word. The stages of this register are connected*

so that a RESET will set the first stage, and clear the other stages." column 15, lines 64-67 thru column 16, lines 1-11); a Code Store SRAM, bidirectionally communicating with the microcontroller (*"Among the teachings set forth in the present application is a low-power low-voltage Complementary Metal Oxide Semiconductor (CMOS) six-transistor static random access memory (SRAM)..."* column 4, lines 3-6). See also (*"After microcontroller 2404 or 2414 resets module 2400 and waits the 480 microseconds with bus 2402 or 2412 released and detects the presence signal of module 2400, it then serially writes the eight bits 0000 1111 (0F in hexadecimal) forming the read command into the command register of module 2400..."* column 51, lines 4-9); see also (*"A one-to-three wire bidirectional transceiver enables this operation and could be based on converter 2102 by coupling the DATA_ IN and DATA_ OUT to a single mode. The second layer commands and register 2104, decode 2106, and ROM and control 2108 could also be part of a one-to-three wire transceiver, see FIG. 37A. A possible implementation of this transceiver would require a great deal of additional circuitry and signals to control the data direction (i.e. whether the bidirectional D/Q port was configured as an input or an output)."* column 64, lines 53-62); and executable code, loaded onto the Code Store RAM (*"Counter 2810 can be read over the 1-wire bus by a host in a manner similar to reading the RAM of module 2100: the host resets module 2800 (counter 2810 does not reset except by a command in the command register), and then loads the Read Counter command into the command register and then reads the contents of counter 2810."* column 57, lines 26-32); a microcontroller configured to bidirectionally communicate with the register file and the run control register (*"After microcontroller 2404 or 2414 resets module 2400 and waits the 480 microseconds with bus 2402 or 2412 released and detects the presence signal of module 2400, it then serially writes the eight*

bits 0000 1111 (0F in hexadecimal) forming the read command into the command register of module 2400... " column 51, lines 4-9). See also (*"A one-to-three wire bidirectional transceiver enables this operation and could be based on converter 2102 by coupling the DATA_IN and DATA_OUT to a single mode. The second layer commands and register 2104, decode 2106, and ROM and control 2108 could also be part of a one-to-three wire transceiver, see FIG. 37A. A possible implementation of this transceiver would require a great deal of additional circuitry and signals to control the data direction (i.e. whether the bidirectional D/Q port was configured as an input or an output)."* column 64, lines 53-62).

Curry '275 does not expressly disclose a run control register; wherein the Code Store SRAM and the run control register bidirectionally communicates with a system processor; wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.

Smith '733 discloses a run control register (*"The registers 160, 162 and 164 are also coupled to a non-volatile RAM controller 170 which generates a chip select signal for non-volatile RAM 178. Non-volatile RAM 178 is addressed from the SNES address bus and receives write control signal and read control via chip enable as shown in FIG. 7. The contents of boot /run register 164 as well as SNES reset and ROM select signals are coupled to EPROM controller 172 which generates a chip select signal at the appropriate time to read the EPROM 180."* column 13, lines 32-40); wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor (*"As shown in FIG. 6 various power lines and bidirectional control lines are also coupled to the memory board..."*

column 11, lines 54-56). (*"The registers 160, 162 and 164 are also coupled to a non-volatile RAM controller 170 which generates a chip select signal for non-volatile RAM 178. Non-volatile RAM 178 is addressed from the SNES address bus and receives write control signal and read control via chip enable as shown in FIG. 7. The contents of boot /run register 164 as well as SNES reset and ROM select signals are coupled to EPROM controller 172 which generates a chip select signal at the appropriate time to read the EPROM 180. The EPROM controller 172 receives an address from the Super NES address bus. The EPROM may be written in response to an SNES write control signal. Each of the pseudo-static RAM 174, SRAM 176, non-volatile RAM 178 and boot ROM 180 is coupled to the SNES address and data buses."* column 13, lines 32-45); wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code (*"The bits stored in the respective registers are input to a pseudo RAM (PSRAM) controller 166 which, in turn, selects in accordance with the state of the output from registers 158-164, the pseudo RAM 174 address mapping mode. The address mapping functions implemented by the PSRAM controller 166 permits diverse games using different address mapping modes to be executed using the same memory board hardware."* column 13, lines 3-11).

Curry '275 and Smith '733 are combinable because they are from same field of endeavor of communication systems (*"This invention relates generally to digital communications..."* Smith '733 at column 1, lines 18-19).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Curry '275 by adding a run control

register; wherein the Code Store SRAM and the run control register bidirectionally communicates with a system processor; and wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code as taught by Smith '733.

The motivation for doing so would have been because it advantageous permit hotel guests to actively participate in video game play or to use other data processing/communication services (*"The present invention on is directed to a video game /communications system which permits hotel guests to actively participate in video game play or to use other data processing/communication services."* Smith '733 at column 5, lines 1-2).

Therefore, it would have been obvious to combine Curry '275 with Smith '733 to obtain the invention as specified in claim 1.

Regarding claim 2; Curry '275 discloses a device wherein the types of the registers are selected from a group that includes timer, General purpose, external I/O, internal I/O, shared, and interrupt (*"Further preferred embodiment circuitry for chips 0130 and 0130' in the modules of FIGS. 1A-B are shown schematically in FIGS. 21, 22A, 22B, 22D, and 22G. FIG. 21 is a top level schematic of the embodiment, denoted generally 2100, which includes a single input-output terminal IO, a 1-wire converter 2102, an 8-bit command shift register 2104, a command decoder 2106, ROM and control 2108, secure RAM 2110, multiplexer 2112, power supply battery 2114, and battery test circuit 2116. Embodiment 2100 receives and transmits serially over the IO terminal..."* column 36, lines 52-56).

Regarding claim 3; Curry '275 discloses a device wherein when one of the registers has a type of external I/O, the register including edge detect logic (*"FIGS. 9A and 9B are two parts of a single Figure which shows the control logic used, in the presently preferred embodiment, in the integrated circuit of FIG. 6. After the protocol register 920 has been loaded, counter chain 910 counts successive clock pulses. (Every falling edge on the data line will lead to a clock pulse within the module, and these pulses are counted by counter 920.) The counter 910 is also connected to logic which will intercept the clock signal (to freeze the count), and activate signal 210, as soon as 256 bits of data have been read or written. (Note that the counter chain shown actually includes two more stages than are needed. This permits ready modification for 1024-bit embodiments.) Register 920 receives the protocol word. The stages of this register are connected so that a RESET will set the first stage, and clear the other stages. Thus, when a 1 propagates through to the last stage, a protocol word has been loaded."* column 15, lines 64-67 thru column 16, lines 1-13).

Regarding claim 6; Curry '275 discloses a device wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM (*"To interface to this protocol, the programmable capabilities of the standard UART chip in the computer's RS232 interface are exploited to provide adaptation to the time base requirements of the module. This is done by writing an entire byte of output from the UART, at a much higher*

baud rate than the module can be relied on to accept, to write a single bit of data into the module. The read-data line (RX) of the UART is tied back to the transmit-data line (TX) through a resistor, so that the UART will also always report a read of the same data byte being written, unless the token has turned on its pull-down transistor." column 10, lines 18-28).

5. **Claim 4 & 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Curry '275 and Smith '733 as applied to claim 1 above, and further in view of Smith '733.

Regarding claim 4; Curry '275 and Smith '733 does not expressly disclose a device wherein the register type further includes FIFO registers, operative to communicate with a direct memory access controller.

Smith '733 does discloses a device wherein the register type further includes FIFO registers, operative to communicate with a direct memory access controller (*"Memory board 102 additionally includes a control decoder 182 that is coupled to the SNES address lines. In response to signals received on the SNES address lines, control decoder 182 couples a "data ready" signal to microcontroller 190, a "read" signal to first-in first-out (FIFO) buffer 184, provides a "data shift in" signal to latch 188 (which receives data from the SNES data lines) which, in turn, shifts data out to microcontroller 190. The FIFO 184 receives high speed downloaded information from microcontroller 190 and stores such data in response to the "write" signal generated by MCU 190. The control decoder 182, in response to a read control signal on its input address lines triggers a read operation from FIFO 184. If there is no data available in FIFO 184 upon request, a "data not ready" signal is generated by FIFO 184 which is coupled to control decoder 182 and to the SNES data lines. To write data to MCU 190, the*

SNES processor checks the "busy" line" which indicates if MCU 190 can receive data. If MCU 190 can receive data, then one byte is shifted in latch 188, which, in turn, activates the "Busy" signal by sending a "Input Strobe" signal. If MCU 190 cannot receive data, SNES continues to check the "busy" signal." column 13, lines 61-67 thru column 14, lines 1-15).

Curry '275 and Smith '733 are combinable with Smith '733 because they are from same field of endeavor of communication systems (*"This invention relates generally to digital communications..."* Smith '733 at column 1, lines 18-19).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Curry '275 and Smith '733 by adding a a device wherein the register type further includes FIFO registers, operative to communicate with a direct memory access controller as taught by Smith '733.

The motivation for doing so would have been because it advantageous to permit hotel guests to actively participate in video game play or to use other data processing/communication services (*"The present invention on is directed to a video game /communications system which permits hotel guests to actively participate in video game play or to use other data processing/communication services."* Smith '733 at column 5, lines 1-2).

Therefore, it would have been obvious to combine Curry '275 and Smith '733 with Smith '733 to obtain the invention as specified in claim 1.

Regarding claim 7; Smith '733 discloses a device wherein the system processor is configured to bidirectionally communicate with the register file (*"The computer and memory board are also interconnected via an 8 bit address bus PA0-PA7 which permits addressing of*

registers (described below) that are located in a particular CPU address space." column 12, lines 26-29). See also (*"Commands from the host computer 7 are coupled to the memory board microcontroller and the SNES (which in turn respond to the host computer 7), via this bidirectional link."* column 12, lines 43-46).

6. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Curry '275 and Smith '733 as applied to claim1 above, and further in view of Ueda (US 5,631,637 hereinafter, Ueda '637).

Regarding claim 5; Curry '275 and Smith '733 does not expressly disclose a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface.

Ueda '637 discloses a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface (*"When the printing data of a page are developed in the bit map memory 17, the main control unit 18 sends a printing start signal 121 to a printing mechanism shown in FIG. 2. Said printing mechanism is of so-called raster scanning type, such as a laser beam printer, and releases a horizontal synchronization (BD) signal 122 and a vertical synchronization signal 123 when the printing operation is enabled."* column 4, lines 7-14).

Curry '275 and Smith '733 are combinable with Ueda '637 because they are from same field of endeavor of communication systems (*"The present embodiment has been explained by a configuration employing a laser beam printer, but the present invention is not limited to such configuration and is applicable to any equipment that can effect wireless or cable exchange of*

data with an external equipment, such as a printer of other types, a display apparatus, a memory apparatus or a communication apparatus." Smith '733 at column 6, lines 6-12).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the communication system as taught by Curry '275 and Smith '733 by adding a device wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface as taught by Ueda '637.

The motivation for doing so would have been because it advantageous to provide an output apparatus for receiving data from an external equipment (*"Still another object of the present invention is to provide an output apparatus for receiving data from an external equipment..."* Smith '733 at column 2, lines 3-6).

Therefore, it would have been obvious to combine Curry '275 and Smith '733 with Ueda '637 to obtain the invention as specified in claim 1.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARCUS T. RILEY whose telephone number is (571)270-1581. The examiner can normally be reached on Monday - Friday, 7:30-5:00, est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler L. Haskins can be reached on 571-272-7406. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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